

VERTICAL DUAL GATE FIELD EFFECT TRANSISTOR

ABSTRACT OF THE DISCLOSURE

5 A vertical transistor particularly suitable for
high density integration includes potentially
independent gate structures on opposite sides of a
semiconductor pillar formed by etching or epitaxial
growth in a trench. The gate structure is
surrounded by insulating material which is
selectively etchable to isolation material
surrounding the transistor. A contact is made to
the lower end of the pillar (e.g. the transistor
10 drain) by selectively etching the isolation material
selective to the insulating material. The upper end
of the pillar is covered by a cap and sidewalls of
selectively etchable materials so that gate and
source connection openings can also be made by
15 selective etching with good registration tolerance.
A dimension of the pillar in a direction parallel to
the chip surface is defined by a distance between
isolation regions and selective etching and height
of the pillar is defined by thickness of a
20 sacrificial layer.